

WE CLAIM:

1. A semiconductor device including a contact pad and circuit metallization on the surface of an integrated circuit chip, comprising:

5 a stack of protection layers over the surface of said chip, said stack comprising a first inorganic layer on said surface, a polymer layer on said first inorganic layer, and a second inorganic layer on said polymer layer;

10 a window in said stack of layers exposing said metallization on said integrated circuit chip;

a patterned seed metal layer on said metallization in said window and on said second inorganic layer around said window; and

15 a buffer metal layer positioned on said seed metal layer.

2. The device according to Claim 1 wherein said interconnecting metallization comprises copper.

20 3. The device according to Claim 1 wherein said first inorganic layer comprises silicon nitride.

4. The device according to Claim 1 wherein said first inorganic layer is selected from a group consisting of silicon nitride, silicon oxynitride, silicon carbide, polyimide, and stacked layer of said materials.

25 5. The device according to Claim 1 wherein said first inorganic layer has a thickness in the range from about 0.5 to 2 μ m.

6. The device according to Claim 1 wherein said polymer layer comprises benzocyclobutene or polybenzoxazole.

30 7. The device according to Claim 1 wherein said polymer layer is selected from a group consisting of

polyimides, polyamic acids, polybenzoxazoles, benzocyclobutenes, polybenzocyclobutenes, and polysiloxanes.

8. The device according to Claim 1 wherein said polymer layer has a thickness of the range from about 3 to 10 µm.
- 5 9. The device according to Claim 1 wherein said second inorganic layer comprises silicon dioxide.
- 10 10. The device according to Claim 1 wherein said second inorganic layer is a dielectric selected from a group consisting of silicon dioxide, silicon nitride, silicon oxynitride, and stacked layers thereof.
11. The device according to Claim 1 wherein said second inorganic layer has a thickness from about 0.5 to 2 µm.
- 15 12. The device according to Claim 1 wherein said seed metal comprises copper.
13. The device according to Claim 1 wherein said seed metal overlaps said second inorganic layer by an amount between about 5 and 15 µm.
- 20 14. The device according to Claim 1 wherein said buffer metal comprises a single metal layer.
15. The device according to Claim 14 wherein said single metal layer comprises copper or a copper alloy.
16. The device according to Claim 1 wherein said buffer metal comprises a stack of metal layers.
- 25 17. The device according to Claim 16 wherein said stack of metal layers comprises copper in contact with said seed metal, nickel on top of said copper, and palladium as outermost metal.
- 30 18. The device according to Claim 1 further comprising a metal reflow element attached to said buffer metal.

19. The device according to Claim 1 further comprising a bond wire attached to said buffer metal.

20. A semiconductor device including a contact pad and circuit metallization on the surface of an integrated circuit chip, comprising:

5 a stack of protection layers over the surface of said chip, said stack comprising a first inorganic layer on said surface, a polymer layer on said first inorganic layer, and a second inorganic layer on said polymer layer;

10 a window in said stack of layers exposing said metallization on said integrated circuit chip;

a seed metal layer on said metallization in said window and on said second inorganic layer, said seed metal layer patterned to form an extended trace remote from said window; and

15 a patterned buffer metal layer positioned on a selected location of said seed metal layer.

21. The device according to Claim 20 further comprising a metal reflow element attached to said buffer metal.

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22. The device according to Claim 20 further comprising a bond wire attached to said buffer metal.

23. A wafer-level method for the fabrication of bonding pads on integrated circuit wafers having

25 interconnection metallization, comprising the steps of: depositing over the wafer surface a stack of protection layers comprising:

30 a first layer of inorganic material;

a layer of polymer material over said first inorganic layer; and

a second layer of inorganic material over said polymer layer;

5 patterning said stack of protection layers by
10 opening a plurality of windows in said stack to
15 expose portions of said chip interconnection
metallization;

20 5 depositing a conductive seed layer covering said
patterned stack; and
depositing a buffer metal layer onto said exposed
seed layer.

24. The method according to Claim 23 wherein said step of

10 10 depositing a buffer metal layer comprises depositing a
a buffer metal layer on said seed layer at a location
remote from said window.

25. The method according to Claim 23 wherein said buffer
metal layer comprises a single metallic layer.

15 26. The method according to Claim 25 further comprising the
step of depositing a bump of reflowable metal onto said
buffer metal layer.

27. The method according to Claim 23 wherein said buffer
metal layer comprises a stack of metal layers including
20 20 an outermost bondable metal layer.

28. The method according to Claim 27 further comprising the
step of attaching a bonding wire to said outermost
bondable layer of said stack.

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